# SIMPLE STEP-UP APPARATUS INCLUDING LEVEL SHIFT CIRCUITS CAPABLE OF LOW BREAKDOWN VOLTAGE

## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a step-up apparatus or a DC-DC converter.

### Description of the Related Art

Generally, a step-up apparatus is constructed by a charge pump circuit. On the other hand, in a liquid crystal display (LCD) apparatus, a positive voltage and a negative voltage are required to maintain the quality of the liquid crystal.

A first prior art step-up apparatus for generating a positive voltage and a negative voltage is constructed by a first level shift circuit for receiving a first clock signal to generate two second clock signals opposite in phase with each other, a K (K=2, 3, ···)-multiple charge pump circuit for generating the positive voltage of $K \cdot V_{DD}$ using the second clock signals where $V_{DD}$ is a power supply voltage, a second level shift circuit for receiving the first clock signal to generate two third clock signals opposite in phase with each other, and a (-K)-multiple charge pump circuit for generating the negative voltage of $-K \cdot V_{DD}$ using the third clock signals. This will be explained later in detail.

In the above-described first prior art step-up apparatus, however, since the (-K)-multiple charge pump circuit is complex, the step-up apparatus is high in cost.

A second prior art step-up apparatus for generating a positive voltage and a negative voltage is constructed by a level shift circuit for receiving a clock signal to generate two phase-opposite clock signals, a K(K= 2, 3, ···)-multiple charge circuit for generating the positive voltage of $K \cdot V_{DD}$

using the two phase-opposite clock signals, and a (-1)-multiple charge pump circuit for generating the negative voltage of $-K \cdot V_{DD}$ using the positive voltage and the two phase-opposite clock signals. This also will be explained later in detail.

In the above-described second prior art step-up apparatus, the number of circuit elements is decreased to simplify the apparatus. However, since the transistors within the level shift circuit need to have a much higher breakdown voltage than that of the level shift circuits of the above-described first prior art step-up apparatus, the thickness of gate insulating layers of the transistors, the gate length and/or gate width of the transistors need to be large, which would degrade the integration.

## SUMMARY OF THE INVENTION

It is an object of the present invention to provide a step-up apparatus including level shift circuits capable of a low breakdown voltage.

According to the present invention, in a step-up apparatus, a first level shift circuit receives a first clock signal to generate two phase-opposite second clock signals, and a second level shift circuit receives the first clock signal to generate two phase-opposite third clock signals. A charge pump circuit steps up a power supply voltage at a power supply voltage terminal using the second clock signals to generate a positive voltage, and a polarity inverting circuit inverts the positive voltage using the third clock signals to generate a negative voltage whose absolute value is the same as the positive voltage. A high level of the second clock signals is not higher than the positive voltage, and a low level of the second clock signals is not lower than a voltage at a ground terminal. A high level of the third clock signals

is not higher than the power supply voltage, and a low level of the third clock signals is not lower than the negative voltage.

Also, in a step-up apparatus, a first level shift circuit receives a first clock signal to generate two phase-opposite second clock signals, and a second level shift circuit receives the first clock signal to generate a third clock signal. A charge pump circuit steps up a power supply voltage at a power supply voltage terminal using the second clock signals to generate a positive voltage. A polarity inverting circuit inverts the positive voltage using the third clock signal to generate a negative voltage whose absolute value is the same as the positive voltage. A high level of the second clock signals is not higher than the positive voltage, and a low level of the second clock signals is not lower than a voltage at a ground terminal. A high level of the third clock signal is not higher than the voltage at the ground voltage, and a low level of the third clock signal is not lower than the negative voltage.

Further in a step-up apparatus, a level shift circuit receives a first clock signal to generate a 2nd clock signal, a 3rd clock signal, ···, a K-th clock signal (K= 2, 3, ···) having a definite voltage swing. A charge pump circuit steps up a power supply voltage at a power supply voltage terminal using said first, second, ···, K-th clock signals to generate a positive voltage.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description set forth below, ad compared with the prior art, with reference to the accompanying drawings, wherein:

Fig. 1 is a block circuit diagram illustrating a first

prior art step-up apparatus;

Figs. 2A, 2B, 2C, 2D and 2E are timing diagrams showing the clock signals of the step-up apparatus of Fig.1 ;

Fig. 3 is a detailed circuit diagram of the level shift circuit of Fig. 1;

Fig. 4 is a detailed circuit diagram of the level shift circuit of Fig. 1;

Fig. 5 is a detailed circuit diagram of the K-multiple charge pump circuit of Fig. 1;

Fig. 6 is a detailed circuit diagram of the (-K)-multiple charge pump circuit of Fig. 1;

Fig. 7 is a block circuit diagram illustrating a second prior art step-up appartus;

Figs. 8A, 8B and 8C are timing diagrams showing the clock signals of the step-up apparatus of Fig.7 ;

Fig. 9 is a detailed circuit diagram of the level shift circuit of Fig. 7;

Fig. 10 is a detailed circuit diagram of the (-1)-multiple charge pump circuit of Fig. 7;

Fig. 11 is a block circuit diagram illustrating a first embodiment of the step-up apparatus according to the present invention;

Figs. 12A and 12B are detail circuit diagrams of the (-1)-multiple charge pump circuit of Fig. 11;

Fig. 13 is a table for explaining the ON gate voltages and OFF gate voltages of the transistors of Figs. 12A and 12B;

Fig. 14 is a block circuit diagram illustrating a second embodiment of the step-up apparatus according to the present invention;

Figs. 15A, 15B, 15C and 15D are timing diagram showing the clock signals of the step-up apparatus of Fig. 14;

Fig. 16 is a detailed circuit diagram of the level shift circuit of Fig. 14;

Fig. 17 is a detailed circuit diagram of the (-1)-multiple charge pump circuit of Fig. 14;

Fig. 18 is a table for explaining the ON gate voltages and OFF gate voltages of the transistors of Fig. 17;

Fig. 19 is a circuit diagram illustrating a first modification of the step-up apparatus of Fig. 10;

Fig. 20 is a circuit diagram of the L-multiple charge pump circuit of Fig. 19;

Fig. 21 is a circuit diagram illustrating a second modification of the step-up apparatus of Fig. 10;

Fig. 22 is a circuit diagram of the K-multiple charge pump circuit of Fig. 21;

Fig. 23 is a circuit diagram illustrating a first modification of the step-up apparatus of Fig. 14;

Fig. 24 is a circuit diagram illustrating a second modification of the step-up apparatus of Fig. 14;

Fig. 25 is a circuit diagram illustrating a modification of the level shift circuit and the K-multiple charge pump circuit of Figs. 11 and 14;

Figs. 26A, 26B, 26C, 26D and 26E are timing diagrams showing the clock signals of Fig. 25;

Fig. 27 is a detailed circuit diagram of the level shift circuit of Fig. 25;

Fig. 28 is a block circuit diagram illustrating a third embodiment of the step-up apparatus according to the present invention;

Fig. 29 is a detailed circuit diagram of the K-multiple charge pump circuit of Fig. 28;

Fig. 30 is a table for explaining the ON gate voltages and OFF gate voltages of the transistors of Fig. 29; and

Fig. 31 is a circuit diagram of the step-up apparatus of Fig. 28 applied to an LCD apparatus.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before the description of the preferred embodiments, prior art step-up apparatuses will be explained with reference to Figs. 1, 2A, 2B, 2C, 2D, 2E, 3, 4, 5, 6, 7, 8A, 8B, 8C, 9 and 10.

In Fig. 1, which illustrates a first prior art step-up apparatus for generating a positive voltage of $K \cdot V_{DD}$ ($K=2, 3, \cdots$) and a negative voltage of $-K \cdot V_{DD}$, a level shift circuit 1 is powered by the ground voltage GND and the positive voltage $K \cdot V_{DD}$ to level-shift a clock signal $\phi 0$ having a voltage swing $V_{DD}$ as shown in Fig. 2A, and thus generates clock signals $\phi 1$ and $\overline{\phi 1}$ having a voltage swing $K \cdot V_{DD}$ as shown in Figs. 2B and 2C. On the other hand, a level shift circuit 2 is powered by the negative voltage $-K \cdot V_{DD}$ and the positive voltage $V_{DD}$ to level-shift the clock signal $\phi 0$ having the voltage swing $V_{DD}$ as shown in Fig. 2A, and thus generates clock signals $\phi 2$ and $\overline{\phi 2}$ having a voltage swing $(K+1) \cdot V_{DD}$ as shown in Figs. 2D and 2E.

A K-multiple charge pump circuit 3 steps up the positive voltage $V_{DD}$ using the clock signals $\phi 1$ and $\overline{\phi 1}$ to generate the positive voltage $K \cdot V_{DD}$. On the other hand, a $(-K)$-multiple charge pump circuit 4 steps up the positive voltage $V_{DD}$ using the clock signals $\phi 2$ and $\overline{\phi 2}$ to generate the negative voltage $-K \cdot V_{DD}$.

The voltage $K \cdot V_{DD}$ and $-K \cdot V_{DD}$ are held in capacitors 5 and 6, respectively.

In Fig. 3, which is a detailed circuit diagram of the level shift circuit 1 of Fig. 1, a CMOS level shifter formed by cross-coupled load P-channel MOS transistors 101 and 102 and drive N-channel MOS transistors 103 and 104 is powered by the ground voltage GND and the positive voltage $K \cdot V_{DD}$. The gate of the transistor 103 receives the clock signal $\phi 0$ while the gate of the transistor 104 receives an inverted signal of

the clock signal $\phi 0$ via a CMOS inverter 105. As a result, the CMOS level shifter generates clock signals $\phi 1$ and $\overline{\phi 1}$ having the voltage swing of $K \cdot V_{DD}$ via CMOS inverters 106 and 107. In this case, the CMOS inverters 105, 106 and 107 are powered by the ground voltage GND and the positive voltage $K \cdot V_{DD}$. Therefore, the transistors within the level shift circuit 1 need to have a breakdown voltage higher than $K \cdot V_{DD}$.

In Fig. 4, which is a detailed circuit diagram of the level shift circuit 2 of Fig. 1, a CMOS level shifter formed by cross-coupled load N-channel MOS transistors 201 and 202 and drive P-channel MOS transistors 203 and 204 is powered by the negative voltage $-K \cdot V_{DD}$ and the positive voltage $V_{DD}$. The gate of the transistor 203 receives the inverted signal of the clock signal $\phi 0$ via a CMOS inverter 205 while the gate of the transistor 204 receives the inverted signal $\overline{\phi 0}$. As a result, the CMOS level shifter generates clock signals $\phi 2$ and $\overline{\phi 2}$ having the voltage swing of $(K+1) \cdot V_{DD}$ via CMOS inverters 206 and 207. In this case, the inverters 205, 206 and 207 are powered by the negative voltage $-K \cdot V_{DD}$ and the positive voltage $V_{DD}$. Therefore, the transistors within the level shift circuit 2 need to have a breakdown voltage higher than $(K+1) \cdot V_{DD}$.

In Fig. 5, which is a detailed circuit diagram of the K-multiple charge pump circuit 3 of Fig. 1, the K-multiple charge pump circuit 3 is constructed by circuits 31, 32, 33, ···, 3K. The circuit 31 is formed by a step-up P-channel MOS transistor 311. On the other hand, the circuits 32, 33, ···, 3K have the same configuration. That is, the circuit 3i (i = 2, 3, ···, K) is formed by a charging capacitor 3i1, a charging N-channel MOS transistor 3i2, a charging P-channel MOS transistor 3i3 and a step-up P-channel transistor 3i4.

The operation of the K-multiple charge pump circuit 3 is explained next.

First, when the clock signal $\phi 1$ is made high (=K ·

$V_{DD}$) and the clock signal $\overline{\phi 1}$ is made low (=0V), the charging transistors 322, 323, 332, 333, ···, 3K2 and 3K3 are turned ON, so that the voltages at nodes $N_2$, $N_3$, ···, and $N_K$ of the circuits 32, 33, 3K are made $V_{DD}$. Thus, the capacitors 321, 331, ···, 3K1 are positively charged by $V_{DD}$. Note that the voltage at node $N_1$ of the circuit 31 is always $V_{DD}$.

Next, when the clock signal $\phi 1$ is made low (=0V) and the clock signal $\overline{\phi 1}$ is made high ($K \cdot V_{DD}$), the charging transistors 322, 323, 332, 333, ···, 3K2 and 3K3 are turned OFF, while the step-up transistors 311, 324, 334, ···, and 3K4 are turned ON. As a result, the circuit 31 generates a positive voltage of $V_{DD}$. In the circuit 32, $V_{DD}$ is added to the voltage $V_{DD}$ at node $N_2$, so that the voltage at node $N_2$ becomes $2 \cdot V_{DD}$ ($= V_{DD} + V_{DD}$). Thus, the circuit 32 generates a voltage of $2 \cdot V_{DD}$. In the circuit 32, $2 \cdot V_{DD}$ is added to the voltage $V_{DD}$ at node $N_2$, so that the voltage at node $N_2$ becomes $3 \cdot V_{DD}$ ($= V_{DD} + 2 \cdot V_{DD}$). Thus, the circuit 32 generates a voltage of $3 \cdot V_{DD}$. In the circuit 3K, $(K-1) \cdot V_{DD}$ is added to the voltage $V_{DD}$ at node $N_2$, so that the voltage at node $N_2$ becomes $K \cdot V_{DD}$ ($= V_{DD} + (K-1) \cdot V_{DD}$). Thus, the circuit 3K generates a voltage of $K \cdot V_{DD}$.

In Fig. 6, which is a detailed circuit diagram of the (-K)-multiple charge pump circuit 4 of Fig. 1 (see: Fig. 10 of JP-A-6-165482 where a (-2)-multiple charge pump circuit is disclosed), the (-K)-multiple charge pump circuit 4 is constructed by circuits 40, 41, 42, ···, 4K. The circuit 40 is formed by a step-up N-channel MOS transistor 401. On the other hand, the circuits 41, 42, ···, 4K have the same configuration. That is, the circuit 4i (i = 1, 2, ···, K) is formed by a charging capacitor 4i1, a charging P-channel MOS transistor 4i2, a charging N-channel MOS transistor 4i3 and a step-up N-channel transistor 4i4.

The operation of the (-K)-multiple charge pump

circuit 4 is explained next.

First, when the clock signal $\phi 2$ is made low (= $-K \cdot V_{DD}$) and the clock signal $\overline{\phi 2}$ is made high (= $V_{DD}$), the charging transistors 412, 413, 422, 423, ···, 4K2 and 4K3 are turned ON, so that the voltages at nodes $N_1$, $N_2$, ···, and $N_K$ of the circuit 41, 42, ···, 4K are made $V_{DD}$. Thus, the capacitors 411, 421, ···, 4K1 are negatively charged by $V_{DD}$.

Next, when the clock signal $\phi 2$ is made low (= $-K \cdot V_{DD}$) and the clock signal $\overline{\phi 2}$ is made high (= $V_{DD}$), the charging transistors 412, 413, 422, 423, ···, 4K2 and 4K3 are turned OFF, while the step-up transistors 401, 414, 424, ···, and 4K4 are turned ON. As a result, the circuit 40 generates the ground voltage 0V. In the circuit 41, $-V_{DD}$ is added to the voltage 0V at node $N_1$, so that the voltage at node $N_1$ becomes $-V_{DD}$ (= $0 - V_{DD}$). Thus, the circuit 41 generates a voltage of $-V_{DD}$. In the circuit 42, $(-V_{DD} - V_{DD})$is added to the voltage 0V at node $N_2$, so that the voltage at node $N_2$ becomes $-2 \cdot V_{DD}$ (=$0 - V_{DD} - V_{DD}$). Thus, the circuit 32 generates a voltage of $-2 \cdot V_{DD}$. In the circuit 4K, $-(K-1) \cdot V_{DD} - V_{DD}$ is added to the voltage 0V at node $N_2$, so that the voltage at node $N_2$ becomes $-K \cdot V_{DD}$ (= $0V - (K-1) \cdot V_{DD} - V_{DD}$). Thus, the circuit 4K generates a voltage of $-K \cdot V_{DD}$.

In the push-up apparatus of Fig. 1, however, since the (-K)-multiple charge pump circuit 4 is complex, the step-up apparatus of Fig. 1 is high in cost.

In Fig. 7, which illustrates a second prior art step-up apparatus, the level shift circuit 1 of Fig. 1 is deleted, and the level shift circuit 2 of Fig. 1 is modified to a level shift circuit 2A. Also, a (-1)-multiple charge pump circuit (or a polarity inverting circuit ) 7 is provided instead of the (-K)-multiple charge pump circuit 4 of Fig. 1 (see: Fig. 13 of JP-A-6-165482 where K=2).

The level shift circuit 2A is powered by a negative

voltage $-K \cdot V_{DD}$ and a positive voltage $K \cdot K_{DD}$ to level-shift a clock signal $\phi 0$ having a voltage swing $V_{DD}$ as shown in Fig. 8A to generate clock signals $\phi 3$ and $\overline{\phi 3}$ having a voltage swing $2K \cdot V_{DD}$ as shown in Figs. 8B and 8C.

In Fig. 9, which is a detailed circuit diagram of the level shift circuit 2A of Fig. 7, a first CMOS level shifter formed by cross-coupled load P-channel MOS transistors 201a and 202a and N-channel drive MOS transistors 203a and 204a is powered by the negative voltage $-K \cdot V_{DD}$ and the positive voltage $K \cdot V_{DD}$, and also, a second CMOS level shifter formed by cross-coupled load N-channel MOS transistors 205a and 206a and drive P-channel drive MOS transistors 207a and 208a is powered by the negative voltage $-K \cdot V_{DD}$, and the positive voltage $K \cdot V_{DD}$. The gate of the transistor 203a receives the clock signal $\phi 0$ while the gate of the transistor 204a receives an inverted signal of the clock signal $\phi 0$ via a CMOS inverter 209a. Also, the gate of the transistor 207a receives a voltage at the drain of the transistor 201a while the gate of the transistor 208a receives a voltage at the drain of the transistor 202a. As a result, the second CMOS level shifter generates clock signals $\phi 3$ and $\overline{\phi 3}$ having a voltage swing $2K \cdot V_{DD}$ via CMOS inverters 210a and 211a. In this case, the inverters 209a, 210a and 211a are powered by the negative voltage $-K \cdot V_{DD}$ and the positive voltage $K \cdot V_{DD}$. Therefore, in the transistors within the level shift circuit 2A need to have a breakdown voltage higher than $2K \cdot V_{DD}$.

In Fig. 10, which is a detailed circuit diagram of the (-1)-multiple charge pump circuit 7 of Fig. 7, the (-1)-multiple charge pump circuit 7 is constructed by a charging capacitor 701, a charging P-channel MOS transistor 702, a charging N-channel MOS transistor 703, a step-up N-channel MOS transistor 704 and a step-up N-channel MOS transistor 705.

The operation of the (-1)-multiple charge pump circuit 7 of Fig. 10 is explained next.

First, when the clock signal $\phi 3$ is made low ($=-K \cdot V_{DD}$) and the clock signal $\overline{\phi 3}$ is made high ($= K \cdot V_{DD}$), the transistors 702 and 703 are turned ON, so that the capacitor 701 is charged by $2 \cdot V_{DD}$.

Next, when the clock signal $\phi 3$ is made high ($= K \cdot V_{DD}$) and the clock signal $\overline{\phi 3}$ is made low($-K \cdot V_{DD}$), the charging transistors 702 and 703 are turned OFF, while the step-up transistors 704 and 705 are turned ON. As a result, the (-1)-multiple charge pump circuit 7 generates the voltage $-K \cdot V_{DD}$ which is stored in the capacitor 6 of Fig. 7.

In the step-up apparatus of Fig. 7, although the number of circuit elements is decreased to simplify the apparatus, the transistors within the level shift circuit 2A need to have a breakdown voltage higher than $2K \cdot V_{DD}$, which increases the thickness of gate insulating layers, the gate length and/or width of gate electrodes of the transistors, thus degrading the integration of the apparatus.

In Fig. 11, which illustrates a first embodiment of the step-up apparatus according to the present invention, the (-K)-multiple charge pump circuit 4 of Fig. 1 is replaced by a (-1)-multiple charge pump circuit (or a polarity inverting circuit) 7A which receives the positive voltage $K \cdot V_{DD}$ from the K-multiple charge pump circuit 3 to generate a negative voltage $-K \cdot V_{DD}$ using the clock signals $\phi 1$, $\phi 2$ and $\overline{\phi 2}$.

The (-1)-multiple charge pump circuit 7A is illustrated in detail in Figs. 12A and 12B which correspond to Fig. 10.

In Fig. 12A, the gates of the transistors 702 and 704 receive the clock signal $\phi 1$. On the other hand, the gate of the transistor 705 receives the clock signal $\phi 2$ while the gate of the transistor 703 receives the clock signal $\overline{\phi 2}$. That

is, as shown in Fig. 13, the transistor 702 can be switched between a gate voltage of $K \cdot V_{DD} - |V_{tp}|$ and a gate voltage of $K \cdot V_{DD}$, and the transistor 704 can be switched between a gate voltage of 0V and a gate voltage of $V_{tn}$. Note that $V_{tp}$ designates a threshold voltage of the P-channel MOS transistors, and $V_{tn}$ designates a threshold voltage of the N-channel MOS transistors. Therefore, the transistors 702 and 704 can be switched between a gate voltage of 0V and a gate voltage of $K \cdot V_{DD}$, so that the transistors 702 and 704 can be switched by the clock signal $\phi 1$. Also, as shown in Fig. 13, the transistor 705 can be switched between a gate voltage of $-K \cdot V_{DD}$ and a gate voltage of $V_{tn} - K \cdot V_{DD}$. Therefore, the transistor 705 can be switched between a gate voltage of $- K \cdot V_{DD}$ and a gate voltage of $V_{DD}$, so that the transistor 705 can be switched by the clock signal $\phi 2$. Further, as shown in Fig. 13, the transistor 703 can be switched between a gate voltage of $- K \cdot V_{DD}$ and a gate voltage of $V_{tn}$. Therefore, the transistor 703 can be switched between a gate voltage of $- K \cdot V_{DD}$ and a gate voltage of $V_{DD}$, so that the transistor 703 can be switched by the clock signal $\overline{\phi 2}$.

In Fig. 12B, the gates of the transistor 702 receive the clock signal $\phi 1$. On the other hand, the gates of the transistors 704 and 705 receive the clock signal $\phi 2$ while the gate of the transistor 703 receives the clock signal $\overline{\phi 2}$. That is, as shown in Fig. 13, the transistor 502 can be switched between a gate voltage of $K \cdot V_{DD} - |V_{tp}|$ and a gate voltage of $K \cdot V_{DD}$. Therefore, the transistor 702 can be switched between a gate voltage of 0V and a gate voltage of $K \cdot V_{DD}$, so that the transistor 702 can be switched by the clock signal $\phi 1$. Also, as shown in Fig. 13, the transistor 705 can be switched between a gate voltage of $-K \cdot V_{DD}$ and a gate voltage of $V_{tn} - K \cdot V_{DD}$, and the transistor 704 can be switched between a gate voltage of 0V and a gate voltage of $V_{tn}$. Therefore, the transistors

704 and 705 can be switched between a gate voltage of $-K \cdot V_{DD}$ and a gate voltage of $V_{DD}$, so that the transistors 704 and 705 can be switched by the clock signal $\phi 2$. Further, as shown in Fig. 13, the transistor 703 can be switched between a gate voltage of $-K \cdot V_{DD}$ and a gate voltage of $V_{tn}$. Therefore, the transistor 703 can be switched between a gate voltage of $-K \cdot V_{DD}$ and a gate voltage of $V_{DD}$, so that the transistor 703 can be switched by the clock signal $\overline{\phi 2}$.

In Fig. 13, note that since $V_{tp}$ is negative, an ON gate voltage of a P-channel MOS transistor is defined by a gate-to-source voltage of the P-channel MOS transistor equal to $|V_{tp}|$, and an OFF gate voltage is defined by a gate-to-source voltage of the P-channel MOS transistor equal to 0V. Similarly, since $V_{tn}$ is positive, an ON gate voltage of an N-channel MOS transistor is defined by a gate-to-source voltage of the N-channel MOS transistor equal to $V_{tn}$, and an OFF gate voltage is defined by a gate-to-source voltage of the N-channel MOS transistor equal to 0V.

Thus, in the step-up apparatus of Fig. 11, although the two level shift circuits 1 and 2 are necessary, the transistors within the level shift circuits do not need to have a very high breakdown voltage and the (-1)-multiple charge pump circuit 5A is simple, which would decrease the apparatus in cost.

In Fig. 14, which illustrates a second embodiment of the step-up apparatus according to the present invention, the level shift circuit 2 of Fig. 11 is replaced by a level shift circuit 2B, and the (-1)-multiple charge pump circuit 7A of Fig. 11 is replaced by a (-1)-multiple charge pump circuit 7B.

The level shift circuit 2B is powered by the negative voltage $-K \cdot V_{DD}$ and the ground voltage GND to level-shift the clock signal $\phi 1$ as shown in Fig. 15A and, thus

generates a clock signal $\phi 4$ as shown in Fig. 15D.

The (-1)-multiple charge circuit 7B steps up the positive voltage $K \cdot V_{DD}$ using the clock signals $\phi 1$ and $\phi 4$ as shown in Figs. 15B and 15D to generate the negative voltage $-K \cdot V_{DD}$.

In Fig. 16, which is a detailed circuit diagram of the level shift circuit 2B of Fig. 14, a capacitor 208 and a diode 209 which also form a (-1)-multiple charge pump circuit or a polarity inverting circuit are added to the elements of the level shift circuit 2 of Fig. 4, and the CMOS inverter 207 of Fig. 4 is deleted. That is, the polarity inverting circuit formed by the capacitor 208 and the diode 209 generates a clock signal $\phi 0'$ having a voltage swing of $V_{DD}$ between $-V_{DD}$ and 0V. As a result, the CMOS level shifter formed by the transistors 203 to 204 generates the clock signal $\phi 4$ via the CMOS inverter 206. In this case, the transistors 203 to 204 and the CMOS inverters 205 and 206 are powered by the negative voltage $-K \cdot V_{DD}$ and the ground voltage GND. Therefore, the transistors within the level shift circuit 2B need to have a breakdown higher then $K \cdot V_{DD}$. In other words, the transistors within the level shift circuit 2B do not need to have a higher breakdown voltage than those within the level shift circuit 2 of Fig. 1, which would improve the integration of the apparatus.

In Fig. 17, which is a detailed circuit diagram of the (-1)-multiple charge pump circuit 7B of Fig. 14, the charging N-channel MOS transistor 703 of Fig. 10 is replaced by a charging P-channel MOS transistor 703'.

In Fig. 17, the gates of the transistors 702 and 704 receive the clock signal $\phi 1$. On the other hand, the gates of the transistors 703' and 725 receive the clock signal $\phi 4$. That is, as shown in Fig. 18, the transistor 702 can be switched between a gate voltage of $K \cdot V_{DD} - |V_{tp}|$ and a gate voltage of $K \cdot V_{DD}$, and the transistor 704 can be switched between a gate

voltage of 0V and a gate voltage of $V_{tn}$. Therefore, the transistors 702 and 704 can be switched between a gate voltage of 0V and a gate voltage of $K \cdot V_{DD}$, so that the transistors 702 and 704 can be switched by the clock signal $\phi 1$. Also, as shown in Fig. 18, the transistor 705 can be switched between a gate voltage of $-K \cdot V_{DD}$ and a gate voltage of $V_{tn} - K \cdot V_{DD}$, and the transistor 703' can be switched between a gate voltage of $-|V_{tp}|$ and a gate voltage of 0V. Therefore, the transistors 703' and 705 can be switched between a gate voltage of $-K \cdot V_{DD}$ and a gate voltage of 0V, so that the transistors 703' and 705 can be switched by the clock signal $\phi 4$.

In Fig. 19, which illustrates a first modification of the step-up apparatus of Fig. 11, this step-up apparatus generates a positive voltage of $L \cdot V_{DD}$ (L=3, 4, ···) and a negative voltage $-K \cdot V_{DD}$ (K=2, 3, ···) where L > K. In this case, the K-multiple charge pump circuit 3 of Fig. 11 is replaced by an L-multiple charge pump circuit 3A as illustrated in Fig. 20. That is, the circuit 3K of Fig. 20 generates the positive voltage $K \cdot V_{DD}$ and transmits it to the (-1)-multiple charge pump circuit 7A. On the other hand, a circuit 3L of Fig. 20 generates a positive voltage $L \cdot V_{DD}$ and transmits it to the level shift circuit 1 and the capacitor 5.

In Fig. 21, which illustrates a second modification of the step-up apparatus of Fig. 11, this step-up apparatus generates a positive voltage of $L \cdot V_{DD}$ (L=2, 3, ···) and a negative voltage $-K \cdot V_{DD}$ (K=3, 4, ···) where L < K. In this case, the K-multiple charge pump circuit 3 of Fig. 11 is replaced by a K-multiple charge pump circuit 3B as illustrated in Fig. 22. That is, a circuit 3L of Fig. 22 generates the positive voltage $L \cdot V_{DD}$ and transmits it to the capacitor 5. On the other hand, a circuit 3K of Fig. 22 generates a positive voltage $K \cdot V_{DD}$ and transmits it to the level shift circuit 1

and the (-1)-multiple charge circuit 7A.

Thus, according to the modifications of the first embodiment as illustrated in Figs. 19 and 21, the absolute values of the positive voltage and the negative voltage can be different from each other.

In Fig. 23, which illustrates a first modification of the step-up apparatus of Fig. 14, this step-up apparatus generates a positive voltage of $L \cdot V_{DD}$ (L=3, 4, ···) and a negative voltage $-K \cdot V_{DD}$ (K=2, 3, ···) where L > K. In this case, the K-multiple charge pump circuit 3 of Fig. 14 is replaced by an L-multiple charge pump circuit 3A as illustrated in Fig. 20. That is, the circuit 3K of Fig. 20 generates the positive voltage $K \cdot V_{DD}$ and transmits it to the (-1)-multiple charge pump circuit 7B. On the other hand, a circuit 3L of Fig. 20 generates a positive voltage $L \cdot V_{DD}$ and transmits it to the level shift circuit 1 and the capacitor 5.

In Fig. 24, which illustrates a second modification of the step-up apparatus of Fig. 14, this step-up apparatus generates a positive voltage of $L \cdot V_{DD}$ (L=2, 3, ···) and a negative voltage $-K \cdot V_{DD}$ (K=3, 4, ···) where L < K. In this case, the K-multiple charge pump circuit 3 of Fig. 14 is replaced by a K-multiple charge pump circuit 3B as illustrated in Fig. 22. That is, a circuit 3L of Fig. 22 generates the positive voltage $L \cdot V_{DD}$ and transmits it to the capacitor 5. On the other hand, a circuit 3K of Fig. 22 generates a positive voltage $K \cdot V_{DD}$ and transmits it to the level shift circuit 1 and the (-1)-multiple charge circuit 7B.

Thus, according to the modifications of the second embodiments as illustrated in Figs. 23 and 24, the absolute values of the positive voltage and the negative voltage can be different from each other.

In Fig. 25, which illustrates a modification of the

level shift circuit 1 and the K-multiple charge pump circuit 3 of Figs. 11 and 14, the level shift circuit 1 of Figs. 11 and 14 is replaced by level shift circuits 12, 13, ···, 1K corresponding to the circuits 32, 33, ···, 3K of the K-multiple charge circuit 3. The level shift circuit 12 receives a clock signal $\phi(1)$ ($=\phi 0$) having a voltage swing of $V_{DD}$ as shown in Fig. 26A to generate a clock signal $\phi(2)$ having a voltage swing of $2 \cdot V_{DD}$ as shown in Fig. 26B. The level shift circuit 13 receives a clock signal $\phi(2)$ to generate a clock signal $\phi(3)$ having a voltage swing of $2 \cdot V_{DD}$ as shown in Fig. 26C. Generally, the level shift circuit 1i (i=4, 5, ···, K) receives a clock signal $\phi$ (i-1) having a voltage swing of $2 \cdot V_{DD}$ between $(i-3) \cdot V_{DD}$ and $(i-1) \cdot V_{DD}$ as shown in Fig. 26D to generate a clock signal (i) having a voltage swing of $2 \cdot V_{DD}$ between $(i-2) \cdot V_{DD}$ and $i \cdot V_{DD}$ as shown in Fig. 26E.

Also, in Fig. 25, the P-channel transistors 323, 333, ···, 3K3 of Fig. 5 are replaced by N-channel MOS transistors 323', 333' ···, 3K3', respectively. The gates of the step-up transistors 322, 332, ···, 3K2 are controlled by the clock signal $\phi(1)$ ($=\phi 0$) as shown in Fig. 26A. The gates of the charging transistors 323', 333', ···, 3K3' are controlled by the clock signal $\phi(2)$ as shown in Fig. 26B. The gates of the step-up transistors 324, 334, ···, 3K4 are controlled by the clock signals $\phi(2), \phi(3), \cdots, \phi(K)$, respectively.

The operation of the K-multiple charge pump circuit 3 of Fig. 25 is explained next.

First, when the clock signal $\phi(1)$ is made high ($= V_{DD}$) so that the clock signal $\phi(2)$ is made high ($= 2 \cdot V_{DD}$), the charging transistors 322, 323', 332, 333', 3K2 and 2K3' are surely turned ON, so that the voltages at nodes $N_2$, $N_3$, ···, and $N_K$ of the circuits 32, 33, ···, 3K are made $V_{DD}$. Thus, the capacitors 321, 331, ···, 3K1 are positively charged by $V_{DD}$. Note that the voltage at node $N_1$ of the circuit 31 is always

$V_{DD}$.

In this case, since the clock signals $\phi(2)$, $\phi(3)$, $\cdots$, $\phi(K)$ are at $2 \cdot V_{DD}$, $3 \cdot V_{DD}$, $\cdots$, $K \cdot V_{DD}$, the transistors 324, 334, $\cdots$, 3K4 are surely turned OFF.

Next, when the clock signal $\phi(1)$ is made low (= 0V) so that the clock signal $\phi(2)$ is made low (= 0V), the charging transistors 322, 323', 332, 333', $\cdots$, 3K2 and 3K3' are turned OFF. On the other hand, when the clock signals $\phi(2)$, $\phi(3)$, $\cdots$, $\phi(K)$ are at 0V, $V_{DD}$, $\cdots$, $(K-2) \cdot V_{DD}$, the step-up transistors 324, 324, $\cdots$, 3K4 are turned ON while the step-up transistor 311 is turned ON. As a result, the circuit 31 generates a positive voltage of $V_{DD}$. In the circuit 32, $V_{DD}$ is added to the voltage $V_{DD}$ at node $N_2$, so that the voltage at node $N_2$ becomes $2 \cdot V_{DD}$ $(= V_{DD} + V_{DD})$. Thus, the circuit 32 generates a voltage of $2 \cdot V_{DD}$. In the circuit 32, $2 \cdot V_{DD}$ is added to the voltage $V_{DD}$ at node $N_2$, so that the voltage at node $N_2$ becomes $3 \cdot V_{DD}$ $(= V_{DD} + 2 \cdot V_{DD})$. Thus, the circuit 32 generates a voltage of $3 \cdot V_{DD}$. In the circuit 3K, $(K-1) \cdot V_{DD}$ is added to the voltage $V_{DD}$ at node $N_2$, so that the voltage at node $N_2$ becomes $K \cdot V_{DD}$ $(= V_{DD} + (K-1) \cdot V_{DD})$. Thus, the circuit 3K generates a voltage of $K \cdot V_{DD}$.

Thus, in Fig. 25, the charging transistors 322, 323', 332, 333', $\cdots$, 3K2 and 3K3' are controlled by the clock signal $\phi(1)$ and $\phi(2)$, regardless of their step-up voltages $2 \cdot V_{DD}$, $3 \cdot V_{DD}$, $\cdots$, $K \cdot V_{DD}$. On the other hand, the step-up transistors 311, 324, 334, $\cdots$, 3K4 are controlled by the clock signals $\phi(1)$, $\phi(2)$, $\cdots$, $\phi(K)$, respectively depending on their step-up voltages $V_{DD}$, $2 \cdot V_{DD}$, $3 \cdot V_{DD}$, $\cdots$, $K \cdot V_{DD}$.

In Fig. 27, which is a detailed circuit diagram of the level shift circuit 1i (i= 2, 3, $\cdots$, K) of Fig. 25, a first CMOS level shifter formed by cross-coupled load N-channel MOS transistors 271 and 272 and P-channel drive MOS transistors 273 and 274 is powered by a voltage $(i-2) \cdot V_{DD}$ and a voltage

$(i-1) \cdot V_{DD}$, and also, a second CMOS level shifter formed by cross-coupled load P-channel MOS transistors 275 and 276 and drive N-channel drive MOS transistors 277 and 278 is powered by the voltage $(i-2) \cdot V_{DD}$ and the voltage $i \cdot V_{DD}$. The gate of the transistor 273 receives an inverted signal of the clock signal $\phi(i-1)$ via a CMOS inverter 279 while the gate of the transistor 274 receives the clock signal $\phi(i-1)$. Also, the gate of the transistor 277 receives a voltage at the drain of the transistor 273 while the gate of the transistor 278 receives a voltage at the drain of the transistor 274. As a result, the second CMOS level shifter generates the clock signal $\phi(i)$ having a voltage swing $2K \cdot V_{DD}$ via a CMOS inverter 280. In this case, the CMOS inverter 279 is powered by the voltage $(i-2) \cdot V_{DD}$ and the voltage $(i-1) \cdot V_{DD}$, while the CMOS inverter 280 is powered by the voltage $(i-2) \cdot V_{DD}$ and the voltage $i \cdot V_{DD}$. Therefore, the transistors within the level shift circuit 2 need to have a breakdown voltage higher than $2 \cdot V_{DD}$.

Thus, in Fig. 25, although the number of level shift circuits is increased, the transistors therein do not need to have a high breakdown voltage, thus improving the integration. Additionally, in the level shift circuit as illustrated in Fig. 3 or 4, the power consumption is proportional to $(K \cdot V_{DD})^2$ $(= K^2 \cdot V_{DD}^2)$. On the other hand, in the level shift circuit as illustrated in Fig. 25, the power consumption is proportional to $(K-1) \cdot (2 \cdot V_{DD})^2$ $(= 4(K-1) \cdot V_{DD}^2)$. Therefore, if $K > 3$, the power consumption can be decreased.

In Fig. 28, which illustrates a third embodiment of the step-up apparatus according to the present invention, the clock signals $\phi 2$ and $\overline{\phi 2}$ generated from the level shift circuit 2 of Fig. 11 are also supplied to the K-multiple charge pump circuit 3. In more detail, as illustrated in Fig. 29, which is a detailed circuit diagram of the K-multiple charge

up circuit 3 of Fig. 28, the clock signal $\phi 2$ is supplied to the gate of the P-channel MOS transistor 311 and the clock signal $\overline{\phi 2}$ is supplied to the P-channel MOS transistor 323.

As shown in Fig. 30, all the transistors 311, 322, 323 and 324 can be switched between a gate voltage of 0V and a gate voltage of $K \cdot V_{DD}$. Additionally, the transistors 311 and 323 can be switched between a gate voltage of $-K \cdot V_{DD}$ and a gate voltage of $V_{DD}$. In Fig. 28, use is made of this fact, so that the gate-to-source voltage can be increased to decrease the ON-resistance of the transistors 311 and 323 when they are turned ON.

An example of the push-up apparatus of Fig. 28 applied to a step-up circuit of an LCD apparatus is illustrated in Fig. 31.

In Fig. 31, a voltage $2 \cdot V_{DD}$ is generated from the circuit 32 and stored in a capacitor 5'. The voltage $2 \cdot V_{DD}$ is supplied to a data line driving circuit of the LCD apparatus. On the other hand, a voltage $3 \cdot V_{DD}$ is generated from the circuit 33 and is stored in the capacitor 5. The voltage $3 \cdot V_{DD}$ is supplied to a gate line driving circuit of the LCD apparatus. Also, the voltage $2 \cdot V_{DD}$, not the voltage $3 \cdot V_{DD}$, is supplied to the (-1)-multiple charge pump circuit (polarity inverting circuit) 7A to generate a voltage $-2 \cdot V_{DD}$. The voltage $-2 \cdot V_{DD}$ is supplied to the gate line driving circuit of the LCD apparatus.

As explained hereinabove, according to the present invention, since the breakdown voltage of transistors within the level shift circuits can be lowered, the integration can be improved.